24-Bit Analog-to-Digital Converter with 4-Channel Differential Input Multiplexer

FEATURES

- **240SPS Data Rate with 4MHz Clock**
- **20-Bit Effective Resolution**
- **Input Multiplexer with Four Differential Channels**
- **Pin-Selectable, High-Impedance Input Buffer**
- **±5V Differential Input Range**
- **0.0003% INL (typ), 0.0015% INL (max)**
- **Self-Calibrating**
- **Simple 2-Wire Serial Interface**
- **On-Chip Temperature Sensor**
- **Single Conversions with Standby Mode**
- **Low Current Consumption: 300μA**
- **Analog Supply: 2.7V to 5.5V**
- **Digital Supply: 2.7V to 5.5V**

APPLICATIONS

- **Hand-Held Instrumentation**
- **Portable Medical Equipment**
- **Industrial Process Control**
- **Weigh Scales**

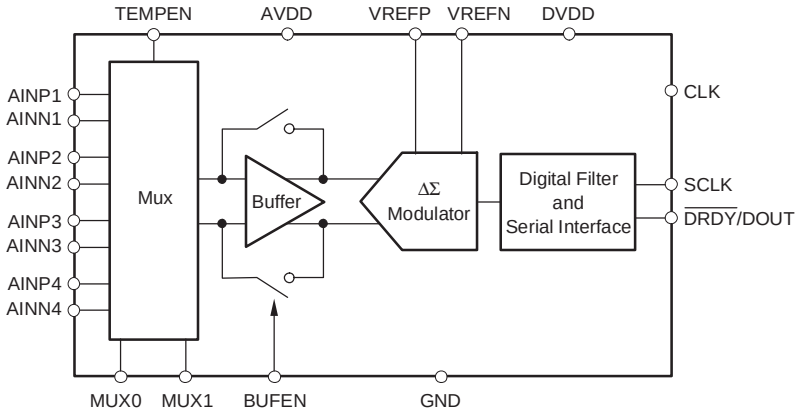
DESCRIPTION

The ADS1224 is a 4-channel, 24-bit, delta-sigma analog-to-digital (A/D) converter. It offers excellent performance and low power in a TSSOP-20 package. The ADS1224 is well-suited for demanding, high-resolution measurements, especially in portable systems and other space-saving and power-constrained applications.

A delta-sigma (ΔΣ) modulator and digital filter form the basis of the A/D converter. The analog modulator has a ±5V differential input range. An input multiplexer (MUX) is used to select between four separate differential input channels. A buffer can be selected to increase the input impedance of the measurement.

A simple, 2-wire serial interface provides all the necessary control. Data retrieval, self-calibration, and Standby mode are handled with a few simple waveforms. When only single conversions are needed, the ADS1224 can be quickly shut down (Standby mode) while idle between measurements to dramatically reduce the overall power consumption. Multiple ADS1224s can be connected together to create a synchronously sampling multichannel measurement system. The ADS1224 is designed to easily connect to microcontrollers, such as the MSP430.

The ADS1224 supports 2.7V to 5.5V analog supplies and 2.7V to 5.5V digital supplies. Power is typically less than 1mW in 3V operation and less than 1μW during Standby mode.



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ORDERING INFORMATION(1)

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1224	TSSOP-20	PW	−40°C to +85°C	ADS1224	ADS1224IPWT	Tape and Reel, 250
					ADS1224IPWR	Tape and Reel, 2500

(1) For the most current specification and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	ADS1224	UNIT
AVDD to GND	−0.3 to +6	V
DVDD to GND	−0.3 to +6	V
Input current	100, momentary	mA
	10, continuous	mA
Analog input voltage to GND	−0.3 to AVDD + 0.3	V
Digital input voltage to GND	−0.3 to DVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	−55 to +125	°C
Storage Temperature Range	−60 to +150	°C
Lead Temperature (soldering, 10s)	+300	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = −40°C to +85°C, AVDD = +5V, DVDD = +5V, f_{CLK} = 2MHz, and V_{REF} = +2.5V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input					
Full-scale input voltage	AINP − AINN		±2V_{REF}		V
Absolute input voltage	Buffer off; AINP, AINN with respect to GND	GND − 0.1		AVDD + 0.1	V
	Buffer on; AINP, AINN with respect to GND	GND + 0.05		AVDD − 1.5	V
Differential input impedance	Buffer off; f_{CLK} = 2MHz		2.7		MΩ
	Buffer on; f_{CLK} = 2MHz		1.2		GΩ
Common-mode input impedance	Buffer off; f_{CLK} = 2MHz		5.4		MΩ
System Performance					
Resolution	No missing codes	24			Bits
Data rate			120 (f_{CLK}/2MHz)		SPS(1)
Integral nonlinearity (INL)	Buffer off, Differential input signal, end point fit		0.0003	0.0015	% of FSR(2)
	Buffer on, Differential input signal, end point fit		0.0006		% of FSR
Offset error	Buffer off		20	100	µV
	Buffer on		20		µV
Offset error drift	Buffer off		0.2		µV/°C
	Buffer on		0.2		µV/°C
Offset error match	Between channels		20	100	µV
Gain error	Buffer off		0.004	0.025	%
	Buffer on		0.008		%
Gain error drift	Buffer off		0.00003		% of FSR/°C
	Buffer on		0.00006		% of FSR/°C
Gain error match	Between channels		0.0005		%
Common-mode rejection	Buffer off, at DC	90	110		dB
	Buffer on, at DC	90	110		dB
Analog power-supply rejection	Buffer off, at DC, ± 10% Δ in AVDD		95		dB
	Buffer on, at DC, ± 10% Δ in AVDD		95		dB
Digital power-supply rejection	Buffer off, at DC, DVDD = 2.7V to 5.5V		85		dB
	Buffer on, at DC, DVDD = 2.7V to 5.5V		85		dB
Noise			0.8		ppm of FSR, rms
Temperature Sensor					
Temperature sensor voltage	T_A = 25°C		106		mV
Temperature sensor coefficient			360		µV/°C
Voltage Reference Input					
Reference input voltage	V_{REF} = VREFP − VREFN	0.5	2.5	AVDD(3)	V
Negative reference input	Buffer off	GND − 0.1		VREFP − 0.5	V
Positive reference input	Buffer off	VREFN + 0.5		AVDD + 0.1	V
Negative reference input	Buffer on	GND + 0.05		VREFP − 0.5	V
Positive reference input	Buffer on	VREFN + 0.5		AVDD − 1.5	V
Voltage reference impedance	f_{CLK} = 2MHz		500		kΩ

(1) SPS = samples per second.
(2) FSR = full-scale range = 4V_{REF}.
(3) It will not be possible to reach the digital output full-scale code when V_{REF} > AVDD/2.

ELECTRICAL CHARACTERISTICS (continued)

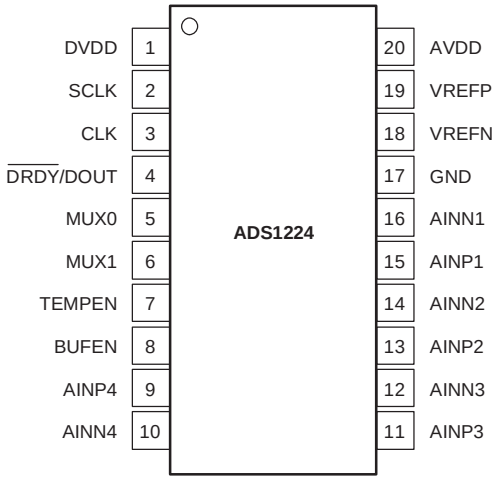
All specifications at T_A = −40°C to +85°C, AVDD = +5V, DVDD = +5V, f_{CLK} = 2MHz, and V_{REF} = +2.5V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input/Output						
Logic levels	V_{IH}		0.8 DVDD		DVDD + 0.1	V
	V_{IL}		GND − 0.1		0.2 DVDD	V
	V_{OH}	I_{OH} = 1mA	0.8 DVDD			V
	V_{OL}	I_{OL} = 1mA			0.2 DVDD	V
Input leakage					±10	µA
CLK frequency (f_{CLK})					8	MHz
CLK duty cycle			30		70	%
Power Supply						
AVDD			2.7		5.5	V
DVDD			2.7		5.5	V
AVDD current		Standby mode		< 1		µA
		AVDD = 5V, normal mode, buffer off		285		µA
		AVDD = 5V, normal mode, buffer on		405		µA
		AVDD = 3V, normal mode, buffer off		265		µA
		AVDD = 3V, normal mode, buffer on		385		µA
DVDD current		Standby mode		< 1		µA
		DVDD = 5V, normal mode		20		µA
		DVDD = 3V, normal mode		10		µA
Total power dissipation		AVDD = DVDD = 5V, buffer off		1.5	2.25	mW
		AVDD = DVDD = 3V, buffer off		0.8		mW
Temperature Range						
Specified			−40		+85	°C
Operating			−55		+125	°C
Storage			−60		+150	°C

(1) SPS = samples per second.
(2) FSR = full-scale range = $4V_{REF}$.
(3) It will not be possible to reach the digital output full-scale code when V_{REF} > AVDD/2.

PIN ASSIGNMENTS

PW PACKAGE
TSSOP
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DVDD	1	Digital	Digital power supply
SCLK	2	Digital input	Serial clock input
CLK	3	Digital input	System clock input
$\overline{\text{DRDY}}$/DOUT	4	Digital Ouput	Dual-purpose output: Data Ready: indicates valid data by going low. Data Output: outputs data, MSB first, on the rising edge of SCLK.
MUX0	5	Digital input	Selects analog input of mux, bit 0
MUX1	6	Digital input	Selects analog input of mux, bit 1
TEMPEN	7	Digital input	Selects temperature sensor input from mux
BUFEN	8	Digital input	Enables input buffer
AINP4	9	Analog input	Analog channel 4 positive input
AINN4	10	Analog input	Analog channel 4 negative input
AINP3	11	Analog input	Analog channel 3 positive input
AINN3	12	Analog input	Analog channel 3 negative input
AINP2	13	Analog input	Analog channel 2 positive input
AINN2	14	Analog input	Analog channel 2 negative input
AINP1	15	Analog input	Analog channel 1 positive input
AINN1	16	Analog input	Analog channel 1 negative input
GND	17	Analog/Digital	Analog and digital ground
VREFN	18	Analog input	Negative reference input
VREFP	19	Analog input	Positive reference input
AVDD	20	Analog	Analog power supply

TYPICAL CHARACTERISTICS

At T_A = −40°C to +85°C, AVDD = +5V, DVDD = +5V, f_{CLK} = 2MHz, and V_{REF} = +2.5V, unless otherwise noted.

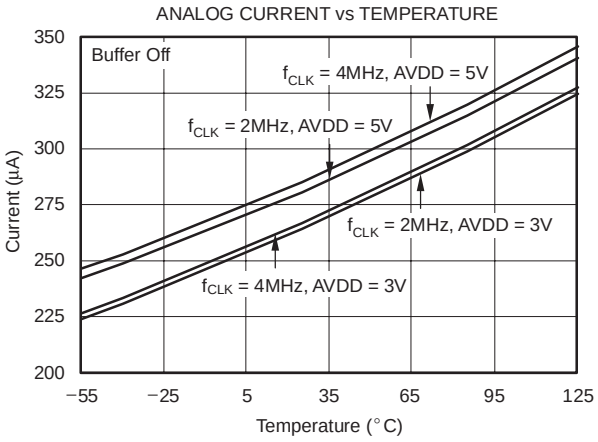

ANALOG CURRENT vs TEMPERATURE
Buffer Off
fCLK = 4MHz, AVDD = 5V
fCLK = 2MHz, AVDD = 5V
fCLK = 2MHz, AVDD = 3V
fCLK = 4MHz, AVDD = 3V
Current (µA)
Temperature (°C)

Figure 1

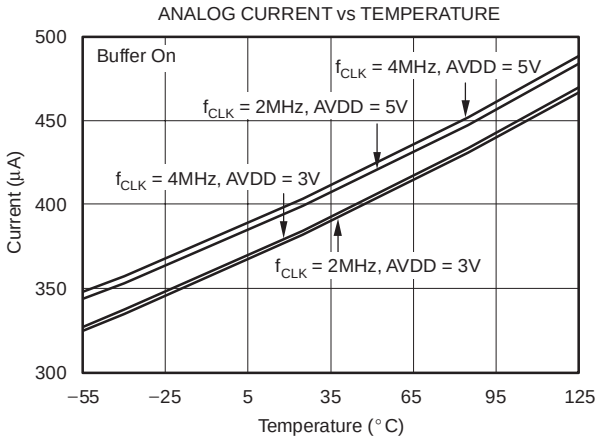

ANALOG CURRENT vs TEMPERATURE
Buffer On
fCLK = 4MHz, AVDD = 5V
fCLK = 2MHz, AVDD = 5V
fCLK = 4MHz, AVDD = 3V
fCLK = 2MHz, AVDD = 3V
Current (µA)
Temperature (°C)

Figure 2

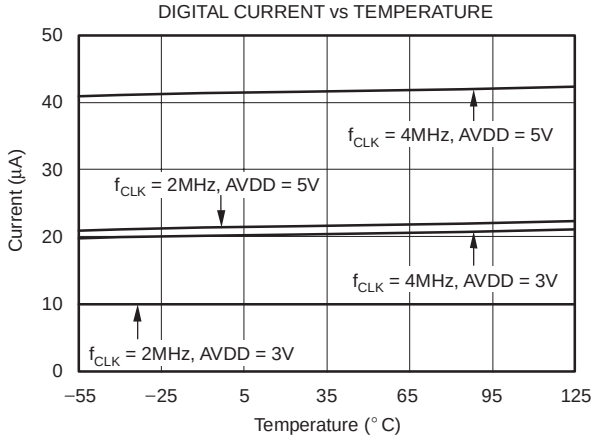

DIGITAL CURRENT vs TEMPERATURE
fCLK = 4MHz, AVDD = 5V
fCLK = 2MHz, AVDD = 5V
fCLK = 4MHz, AVDD = 3V
fCLK = 2MHz, AVDD = 3V
Current (µA)
Temperature (°C)

Figure 3

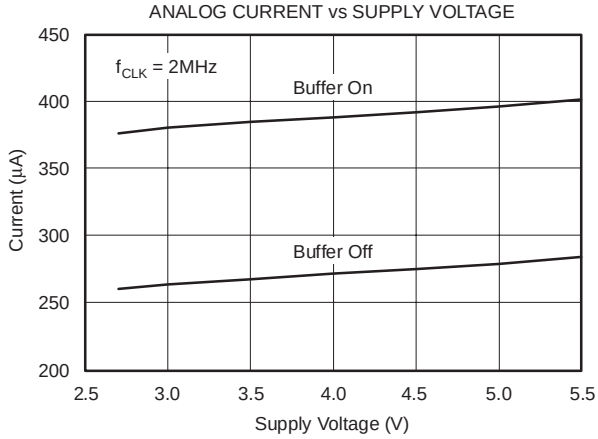


Figure 4

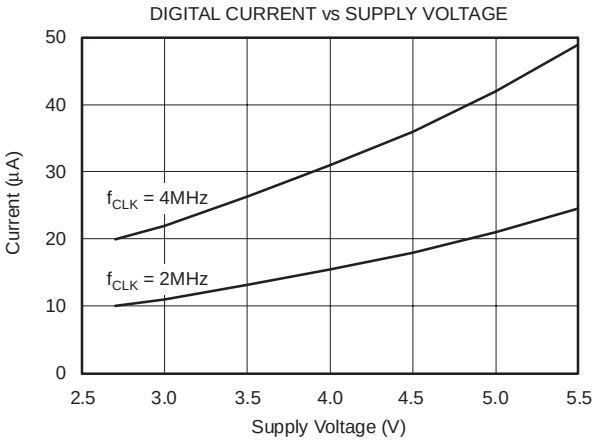


Figure 5

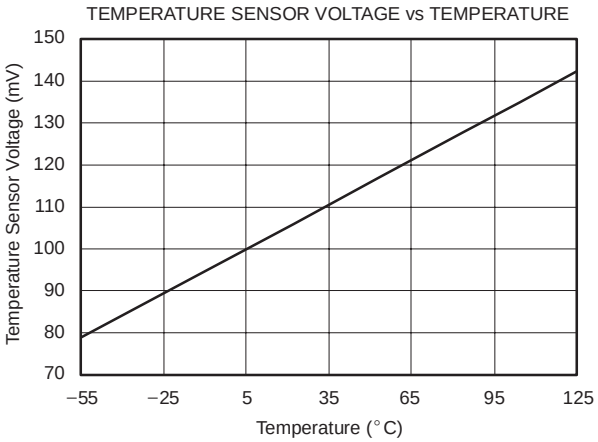


Figure 6

TYPICAL CHARACTERISTICS (CONTINUED)

At T_A = −40°C to +85°C, AVDD = +5V, DVDD = +5V, f_{CLK} = 2MHz, and V_{REF} = +2.5V, unless otherwise noted.

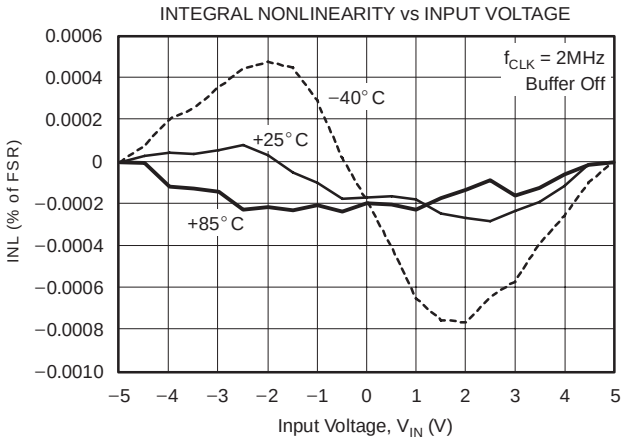


Figure 7

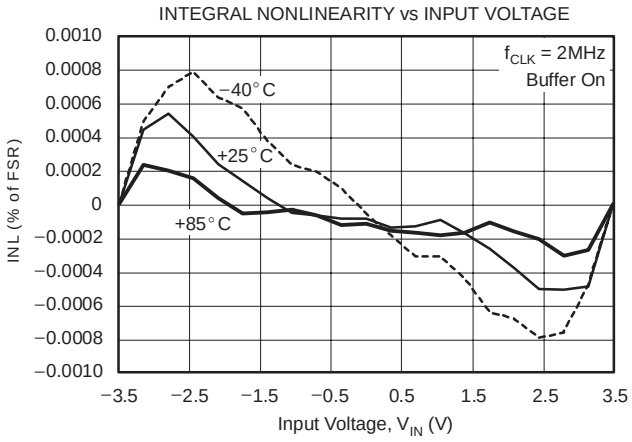


Figure 8

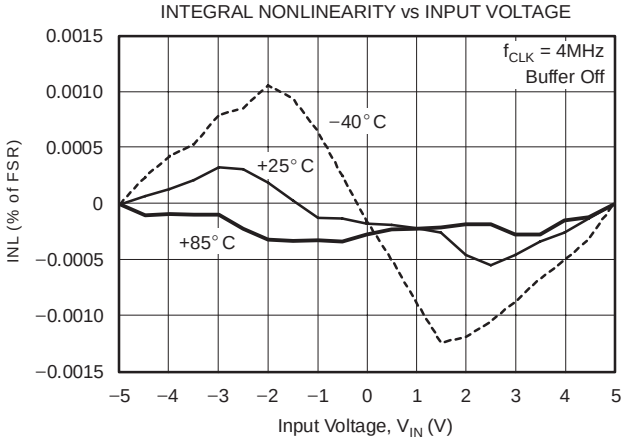


Figure 9

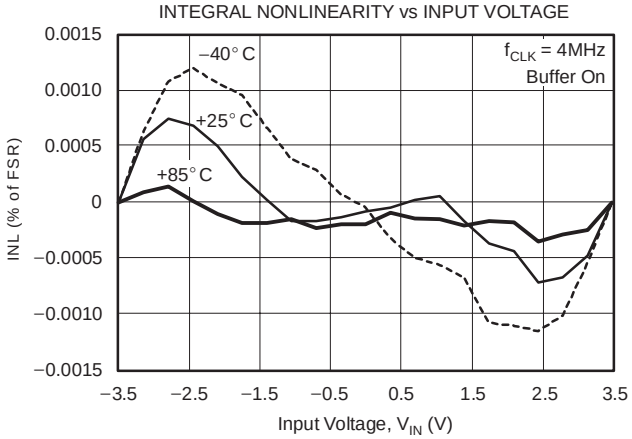


Figure 10

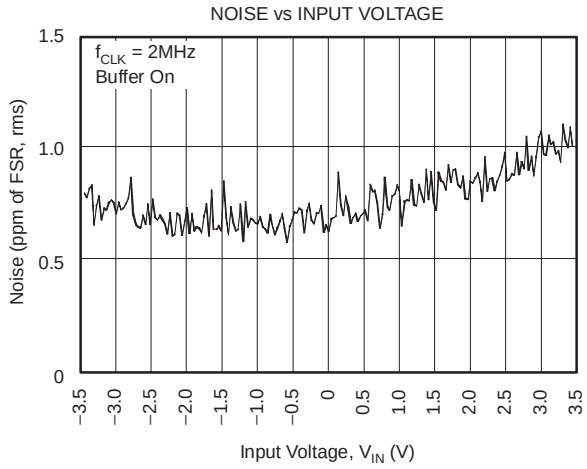


Figure 11

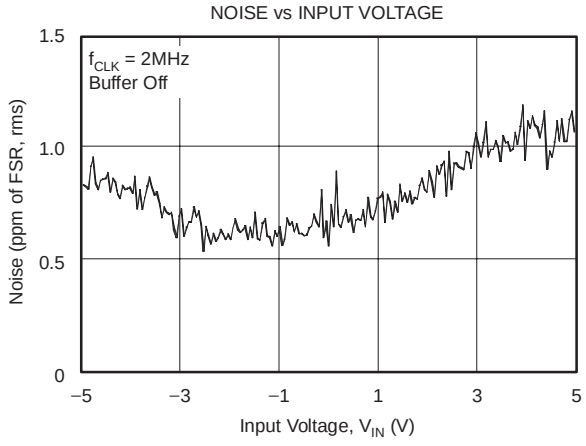


Figure 12

OVERVIEW

The ADS1224 is an A/D converter comprised of a delta-sigma modulator followed by a digital filter. A mux allows for one of four input channels to be selected. A buffer can also be selected to increase the input impedance. The modulator measures the differential input signal V_{IN} = (AINP – AINN) against the differential reference V_{REF} = (VREFP – VREFN). Figure 13 shows a conceptual diagram of the device. The differential reference is scaled internally so that the full-scale input range is $\pm 2V_{REF}$. The digital filter receives the modulator signal and provides a low-noise digital output. A 2-wire serial interface indicates conversion completion and provides the user with the output data.

ANALOG INPUTS (AINPx, AINNx)

The input signal to be measured is applied to the input pins AINPx and AINNx. The positive internal input is generalized as AINP, and the negative internal input is generalized as AINN. The signal is selected though the input mux, which is controlled by pins MUX0 and MUX1, as shown in Table 1. The ADS1224 accepts differential input signals, but can also measure unipolar signals. When measuring unipolar (or single-ended signals) with respect to ground, connect the negative input (AINNx) to ground and connect the input signal to the positive input (AINPx). Note that when the ADS1224 is configured this way, only half of the converter full-scale range is used since only positive digital output codes are produced. An input buffer can be selected to increase the input impedance of the A/D converter with the BUFEN pin.

Table 1. Input Channel selection with MUX0 and MUX1

DIGITAL PINS		SELECTED ANALOG INPUTS	
MUX1	MUX0	POSITIVE INPUT	NEGATIVE INPUT
0	0	AINP1	AINN1
0	1	AINP2	AINN2
1	0	AINP3	AINN3
1	1	AINP4	AINN4

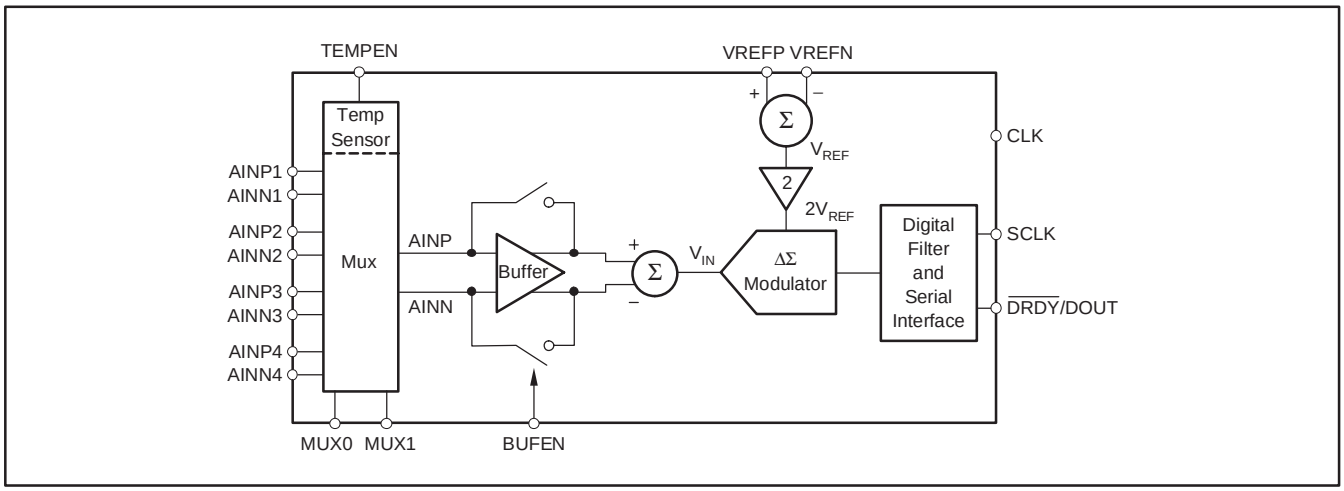


Figure 13. Conceptual Diagram of the ADS1224

Analog Input Measurement without the Input Buffer

With the buffer disabled by setting the BUFEN pin low, the ADS1224 measures the input signal using internal capacitors that are continuously charged and discharged. Figure 14 shows a simplified schematic of the ADS1224 input circuitry, with Figure 15 showing the on/off timings of the switches. The S_1 switches close during the input sampling phase. With S1 closed, C_{A1} charges to AINP, C_{A2} charges to AINN, and C_B charges to (AINP – AINN). For the discharge phase, S_1 opens first and then S_2 closes. C_{A1} and C_{A2} discharge to approximately AVDD/2 and C_B discharges to 0V. This two-phase sample/discharge cycle repeats with a frequency of $f_{CLK}/32$ (62.5kHz for f_{CLK} = 2MHz).

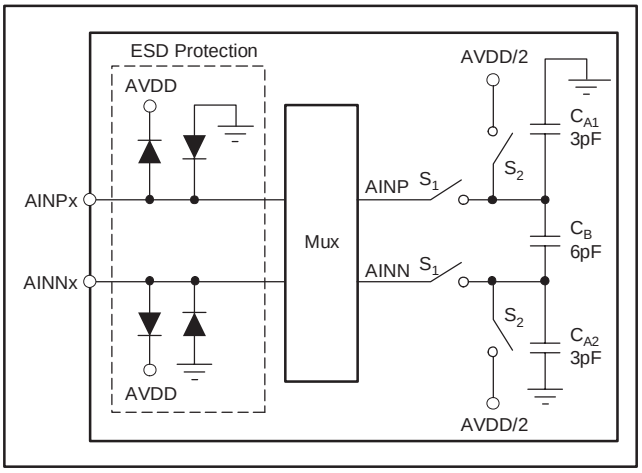


Figure 14. Simplified Input Structure with the Buffer Turned Off

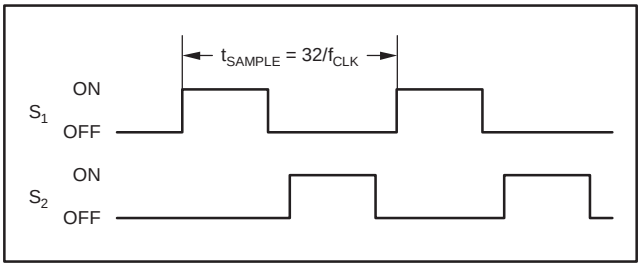


Figure 15. S_1 and S_2 Switch Timing for Figure 14

The constant charging of the input capacitors presents a load on the inputs that can be represented by effective impedances. Figure 16 shows the input circuitry with the capacitors and switches of Figure 14 replaced by their effective impedances. These impedances scale inversely with f_{CLK} frequency. For example, if f_{CLK} frequency is reduced by a factor of 2, the impedances will double.

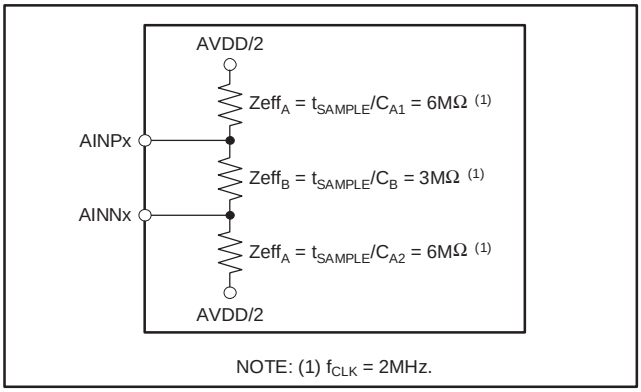


Figure 16. Effective Analog Input Impedances with the Buffer Off

ESD diodes protect the inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below GND by more than 100mV, and likewise do not exceed AVDD by 100mV:

GND – 100mV < (AINP, AINN) < AVDD + 100mV

Analog Input Measurement with the Input Buffer

When the buffer is enabled by setting the BUFEN pin high, a low-drift, chopper-stabilized input buffer is used to achieve very high input impedance. The buffer charges the input sampling capacitors, thus removing the load from the measurement. Because the input buffer is chopper-stabilized, the charging of parasitic capacitances causes the charge to be carried away, as if by resistance. The input impedance can be modeled by a single resistor, as shown in Figure 17. The impedance scales inversely with f_{CLK} frequency, as in the nonbuffered case. Note that during standby mode, the buffer must be disabled to prevent loading of the inputs.

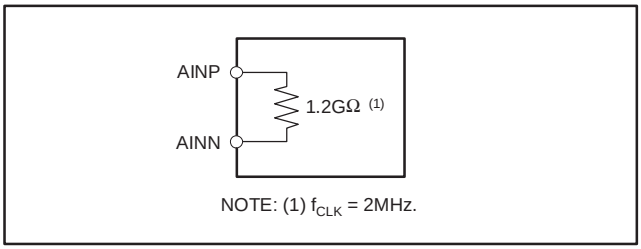


Figure 17. Effective Analog Input Impedances with the Buffer On

Note also that the analog inputs (listed in the Electrical Characteristics table as *Absolute Input Range*) must remain between GND + 0.05V to AVDD − 1.5V. Exceeding this range degrades linearity and results in performance outside the specified limits.

TEMPERATURE SENSOR

On-chip diodes provide temperature-sensing capability. By setting the TEMPEN pin high, the selected analog inputs are disconnected and the inputs to the A/D converter are connected to the anodes of two diodes scaled to 1x and 64x in current and size inside the mux, as shown in Figure 18. By measuring the difference in voltage of these diodes, temperature changes can be inferred from a baseline temperature. Typically, the difference in diode voltages is 106mV at 25°C, with a temperature coefficient of 360µV/°C. A similar structure is used in the MSC1210 for temperature measurement. For more information, see TI application report SBAA100, *Using the MSC121x as a High-Precision Intelligent Temperature Sensor*, available for download at www.ti.com.

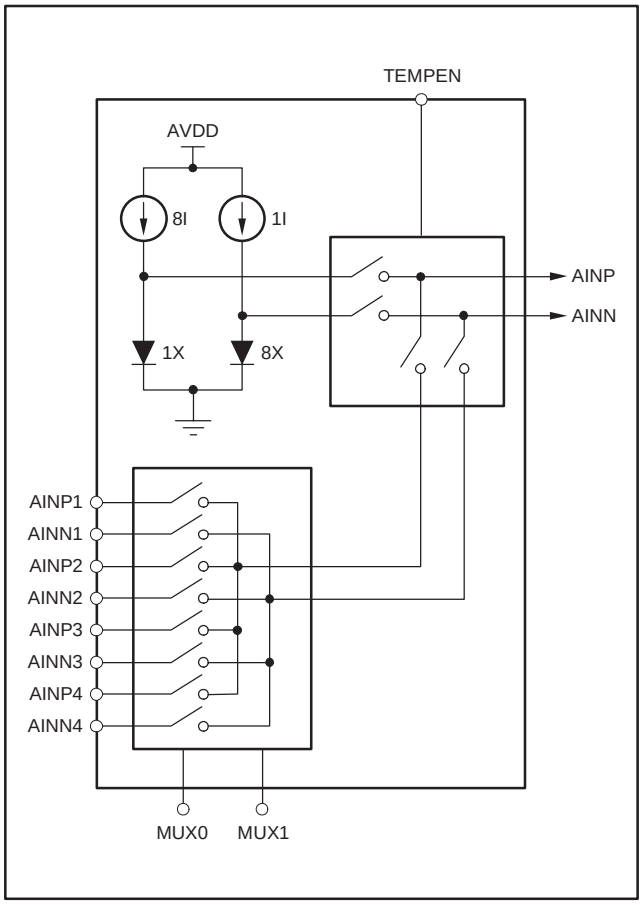


Figure 18. Measurement of the Temperature Sensor in the Input Multiplexer

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference used by the modulator is generated from the voltage difference between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs. A simplified diagram of the circuitry on the reference inputs is shown in Figure 19. The switches and capacitors can be modeled with an effective impedance of:

$$\left(\frac{t_{sample}}{2}\right)/16pF = 500k\Omega$$

where f_{CLK} = 2MHz.

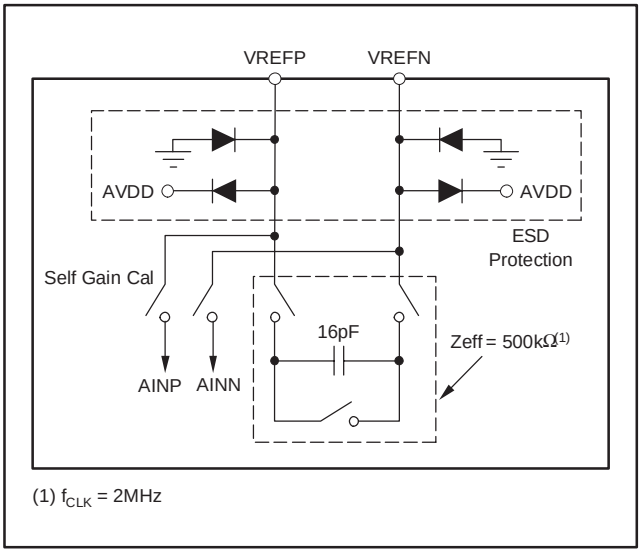


Figure 19. Simplified Reference input Circuitry

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed AVDD by 100mV:

GND – 100mV < (VREFP, VREFN) < AVDD + 100mV

During self gain calibration, all the switches in the input multiplexer are opened, VREFN is internally connected to AINN, and VREFP is connected to AINP. The input buffer may be disabled or enabled during calibration. When the buffer is disabled, the reference pins will be driving the circuitry shown in Figure 9 during self gain calibration, resulting in increased loading. To prevent this additional loading from introducing gain errors, make sure the circuitry driving the reference pins has adequate drive capability. When the buffer is enabled, the loading on the reference pins will be much less, but the buffer will limit the

allowable voltage range on VREFP and VREFN during self or self gain calibration as the reference pins must remain within the specified input range of the buffer in order to establish proper gain calibration.

For best performance, V_{REF} should be AVDD/2, but it can be raised as high as AVDD. When V_{REF} exceeds AVDD/2, it is not possible to reach the full-scale digital output value corresponding to $\pm 2V_{REF}$, since this requires the analog inputs to exceed the power supplies. For example, if V_{REF} = AVDD = 5V, the positive full-scale signal is 10V. The maximum positive input signal that can be supplied before the ESD diodes turn on is when AINP = 5.1V and AINN = –0.1V, resulting in V_{IN} = 5.2V. Therefore, it is not possible to reach the positive (or negative) full-scale readings in this configuration. The digital output codes are limited to approximately one half of the entire range. For best performance, bypass the voltage reference inputs with a 0.1µF capacitor between VREFP and VREFN. Place the capacitor as close as possible to the pins.

CLOCK INPUT (CLK)

This digital input supplies the system clock to the ADS1224. The CLK frequency can be increased to speed up the data rate. CLK must be left running during normal operation. It may be turned off during Standby mode to save power, but this is not required. The CLK input may be driven with 5V logic, regardless of the DVDD or AVDD voltage.

Minimize the overshoot and undershoot on CLK for the best analog performance. A small resistor in series with CLK (10Ω to 100Ω) can often help. CLK can be generated from a number of sources including standalone crystal oscillators and microcontrollers.

DATA READY/DATA OUTPUT ($\overline{\text{DRDY}}$/DOUT)

This digital output pin serves two purposes. First, it indicates when new data is ready by going LOW. Afterwards, on the first rising edge of SCLK, the $\overline{\text{DRDY}}$/DOUT pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data is shifted out on each subsequent SCLK rising edge. After all 24 bits have been retrieved, the pin can be forced high with an additional SCLK. It will then stay high until new data is ready. This is useful when polling on the status of $\overline{\text{DRDY}}$/DOUT to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. As with CLK, this input may be driven with 5V logic regardless of the DVDD or AVDD voltage. There is hysteresis built into this input, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise-and-fall times of SCLK are less than 50ns.

FREQUENCY RESPONSE

The ADS1224 frequency response for f_{CLK} = 2MHz is shown in Figure 20. The frequency response repeats at multiples of the modulator sampling frequency of 62.5kHz. The overall response is that of a low-pass filter with a −3db cutoff frequency of 31.5Hz. As shown, the ADS1224 does a good job attenuating out to 60kHz. For the best resolution, limit the input bandwidth to less than this value to keep higher frequency noise from affecting performance. Often, a simple RC filter on the ADS1224 analog inputs is all that is needed.

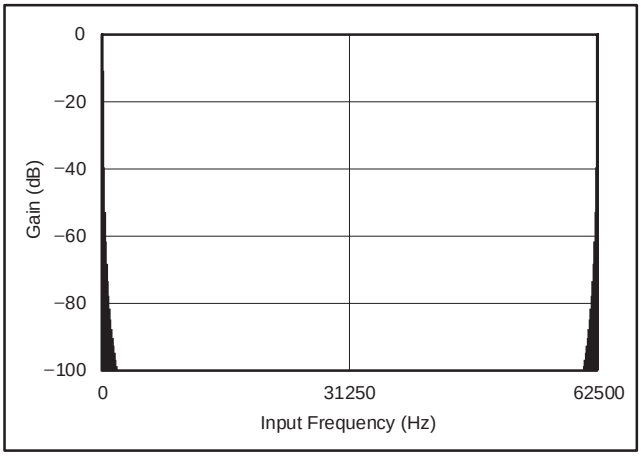


Figure 20. Frequency Response

To help see the response at lower frequencies, Figure 21 illustrates the response out to 1kHz. Notice that signals at multiples of 120Hz are rejected. The ADS1224 data rate and frequency response scale directly with CLK frequency. For example, if f_{CLK} increases from 2MHz to 4MHz, the data rate increases from 120SPS to 240SPS, while the notches increase from 120Hz to 240Hz.

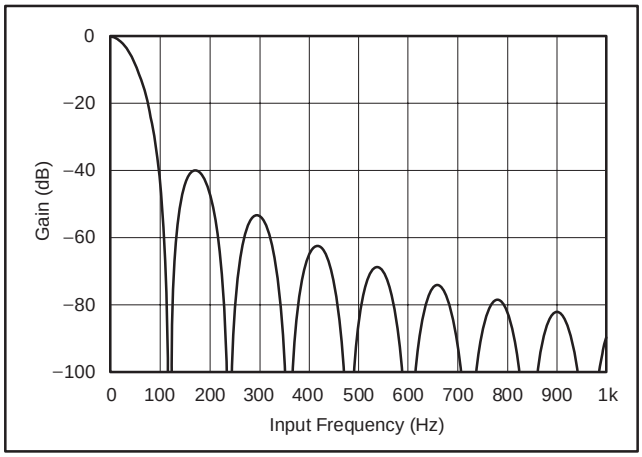


Figure 21. Frequency Response to 1kHz

Rejecting 50Hz or 60Hz noise is as simple as choosing the clock frequency. If simultaneous rejection of 50Hz and 60Hz noise is desired, f_{CLK} = 910kHz can be chosen. The data rate becomes 54.7sps and the frequency response of the ADS1224 rejects the 50Hz and 60Hz noise to below 60dB. The frequency response of the ADS1224 near 50Hz and 60Hz with f_{CLK} = 910kHz is shown in Figure 22.

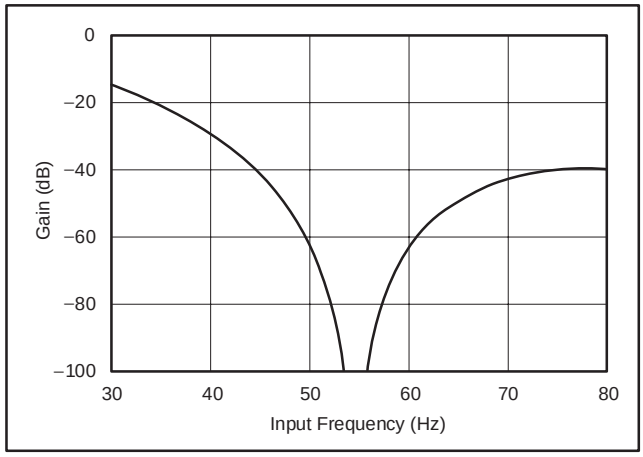
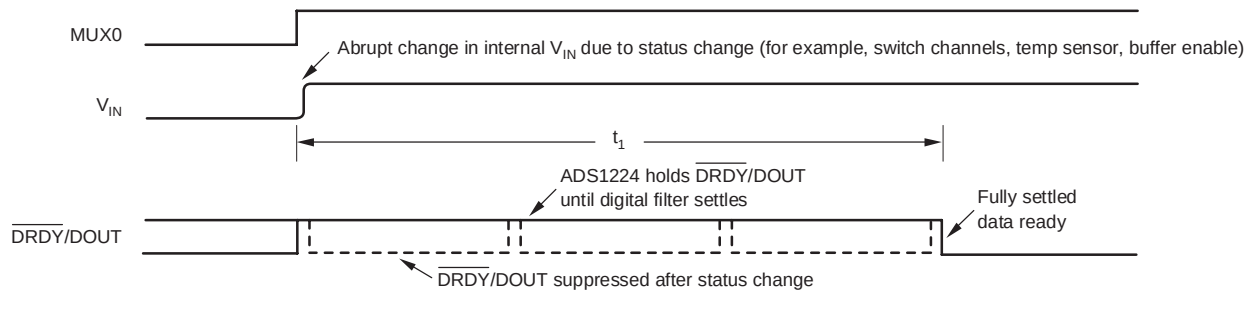


Figure 22. Frequency Response Near 50Hz and 60Hz with f_{CLK} = 910kHz

SETTLING TIME

After changing the input multiplexer, selecting the input buffer, or using temperature sensor, the first data is fully settled. In the ADS1224, the digital filter is allowed to settle after toggling any of the MUX0, MUX1, BUFEN, or TEMPEN pins. Toggling of any of these digital pins will cause the input to switch to the proper channel, start conversions, and hold the $\overline{\text{DRDY}}$/DOUT line high until the digital filter is fully settled. For example, if MUX0 changes from low to high, selecting a different input channel, $\overline{\text{DRDY}}$/DOUT immediately goes high and the conversion process restarts. $\overline{\text{DRDY}}$/DOUT goes low when fully settled data is ready for retrieval. There is no need to discard any data. Figure 23 shows the timing of the DRDY/DOUT line as the input multiplexer changes.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_1(1)	Settling time ($\overline{\text{DRDY}}$/DOUT held high) after a change in any of the MUX0, MUX1, BUFEN, or TEMPEN pins	25.9	26.4	ms

(1) Values given for f_{CLK} = 2MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

Figure 23. Example of Settling Time After Changing the Input Multiplexer

The ADS1224 uses a Sinc^3 digital filter to improve noise performance. Therefore, in certain instances, large changes in input will require settling time. For example, an external multiplexer in front of the ADS1224 can put large changes in input voltage by simply switching input channels. Abrupt changes in the input will require three data cycles to settle. When continuously converting, four readings may be necessary to settle the data. If the change in input occurs in the middle of the first conversion, three more full conversions of the fully settled input will be required to get fully settled data. Discard the first three readings because they will contain only partially−settled data. Figure 24 illustrates the settling time for the ADS1224 in Continuous Conversion mode.

If the input is known to change abruptly, the mux can be quickly switched to an alternate channel and quickly switched back to the original channel. By toggling the mux, the ADS1224 resets the digital filter and initiates a new conversion. During this time, the $\overline{\text{DRDY}}$/DOUT line is held high until fully-settled data is available.

DATA FORMAT

The ADS1224 outputs 24 bits of data in binary two's complement format. The least significant bit (LSB) has a weight of (2VREF)/(2^{23} – 1). The positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 2 summarizes the ideal output codes for different input signals.

Table 2. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} (AINP − AINN)	IDEAL OUTPUT CODE(1)
$\geq +2V_{REF}$	7FFFFFh
$\frac{+2V_{REF}}{2^{23} - 1}$	000001h
0	000000h
$\frac{-2V_{REF}}{2^{23} - 1}$	FFFFFFh
$\leq -2V_{REF}\left(\frac{2^{23}}{2^{23} - 1}\right)$	800000h

(1) Excludes effects of noise, INL, offset, and gain errors.

DATA RETRIEVAL

The ADS1224 continuously converts the analog input signal. To retrieve data, wait until $\overline{\text{DRDY}}$/DOUT goes low, as shown in Figure 25. After this occurs, begin shifting out the data by applying SCLKs. Data is shifted out MSB first. It is not required to shift out all 24 bits of data, but the data must be retrieved before the new data is updated (see t_2) or else it will be overwritten. Avoid data retrieval during the update period. $\overline{\text{DRDY}}$/DOUT remain at the state of the last bit shifted out until it is taken high (see t_6), indicating that new data is being updated. To avoid having $\overline{\text{DRDY}}$/DOUT remain in the state of the last bit, shift a 25th SCLK to force $\overline{\text{DRDY}}$/DOUT high (see Figure 26). This technique is useful when a host controlling the ADS1224 is polling $\overline{\text{DRDY}}$/DOUT to determine when data is ready.

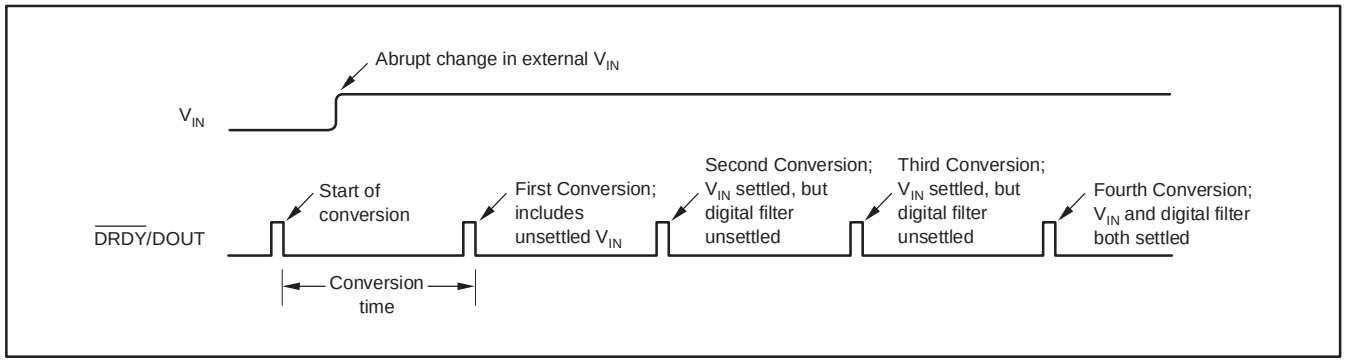
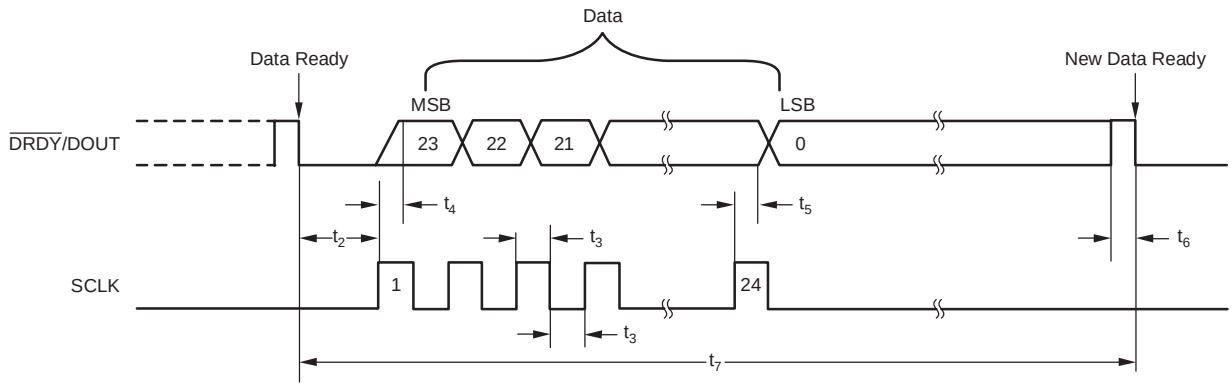

Abrupt change in external V_{IN}
V_{IN}
$\overline{\text{DRDY}}$/DOUT
Start of conversion
First Conversion; includes unsettled V_{IN}
Second Conversion; V_{IN} settled, but digital filter unsettled
Third Conversion; V_{IN} settled, but digital filter unsettled
Fourth Conversion; V_{IN} and digital filter both settled
Conversion time

Figure 24. Settling Time in Continuous Conversion Mode



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_2	$\overline{\text{DRDY}}$/DOUT low to first SCLK rising edge	0		ns
t_3	SCLK positive or negative pulse width	100		ns
t_4(1)	SCLK rising edge to new data bit valid: propogation delay		50	ns
t_5	SCLK rising edge to old data bit valid: hold time	0		ns
t_6(1)	Data updating; no readback allowed	48		µs
t_7(1)	Conversion time (1/data rate)	8.32	8.32	ms

(1) Values given for f_{CLK} = 2MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

Figure 25. Data Retrieval Timing

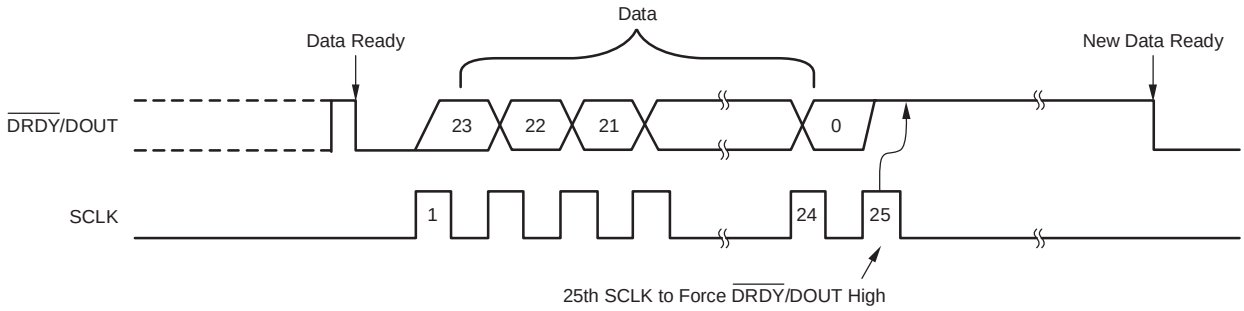


Figure 26. Data Retrieval with $\overline{\text{DRDY}}$/DOUT Forced High Afterwards

SELF-CALIBRATION

Self-calibration can be initiated at any time, although in many applications the ADS1224 drift performance is so good that the self-calibration performed automatically at power-up is all that is needed. To initiate self-calibration, apply at least two additional SCLKs after retrieving 24 bits of data. Figure 27 shows the timing pattern. The 25th SCLK will send $\overline{DRDY}$/DOUT high. The falling edge of the 26th SCLK will begin the calibration cycle. Additional SCLK pulses may be sent after the 26th SCLK; however, activity on SCLK should be minimized during calibration for best results.

When the calibration is complete, $\overline{DRDY}$/DOUT goes low, indicating that new data is ready. There is no need to alter the analog input signal applied to the ADS1224 during calibration; the input pins are disconnected within the A/D converter and the appropriate signals are applied internally and automatically. The first conversion after a calibration is fully settled and valid for use. The time required for a calibration depends on two independent signals: the falling edge of SCLK and an internal clock derived from CLK. Variations in the internal calibration values will change the time required for calibration (t_8) within the range given by the min/max specs. t_{11} and t_{12} described in the next section are affected likewise.

STANDBY MODE

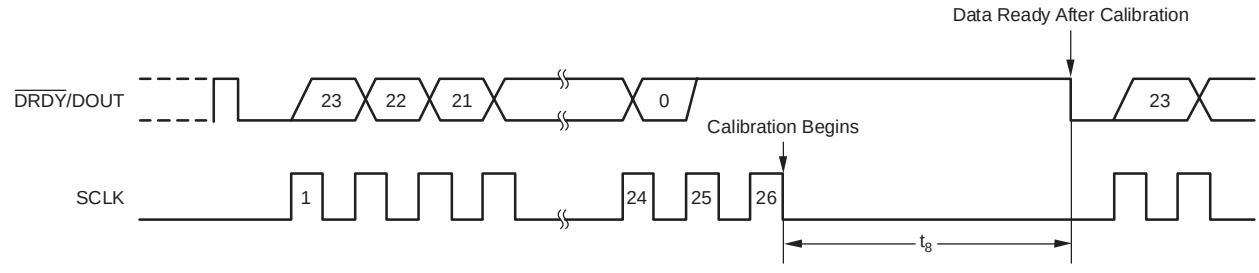
Standby mode dramatically reduces power consumption (typically < 1μW with CLK stopped) by shutting down all of the active circuitry. To enter Standby mode, simply hold SCLK high after $\overline{DRDY}$/DOUT goes low, as shown in Figure 28. Standby mode can be initiated at any time during readback; it is not necessary to retrieve all 24 bits of data beforehand. Note that during standby mode, the buffer must be disabled to prevent loading of the inputs.

When t_{11} has passed with SCLK held high, Standby mode will activate. $\overline{DRDY}$/DOUT stays high when Standby mode begins. SCLK must remain high to stay in Standby mode. To exit Standby mode (wakeup), set SCLK low. The first data after exiting Standby mode is valid. It is not necessary to stop CLK during Standby mode, but doing so will further reduce the digital supply current.

Standby Mode With Self-Calibration

Self-calibration can be set to run immediately after exiting Standby mode. This is useful when the ADS1224 is put in Standby mode for long periods of time and self-calibration is desired afterwards to compensate for temperature or supply voltage changes.

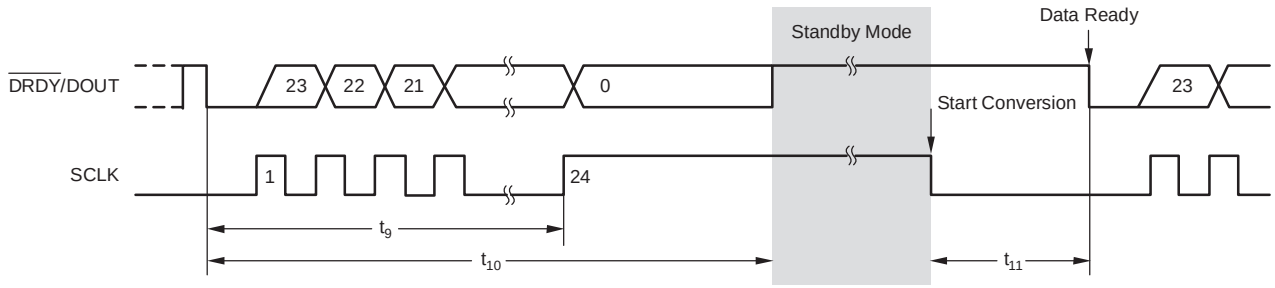
To force a self-calibration with Standby mode, shift 25 bits out before taking SCLK high to enter Standby mode. Self-calibration then begins after wakeup. Figure 29 shows the appropriate timing. Note the extra time needed after wakeup for calibration before data is ready. The first data after Standby mode with self-calibration is fully settled and can be used.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_8(1)	First data ready after calibration	77.1	77.9	ms

(1) Values given for f_{CLK} = 2MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

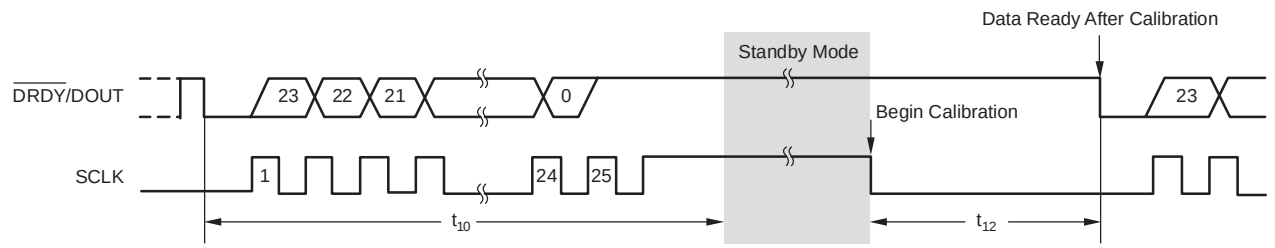
Figure 27. Self-Calibration Timing



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_9(1)	SCLK high after $\overline{\text{DRDY}}$/DOUT goes low to activate Standby mode	0	8.272	ms
t_{10}(1)	Standby mode activation time	8.272	8.304	ms
t_{11}(1)	Data ready after exiting Standby mode	27.7	28.1	ms

(2) Values given for f_{CLK} = 2MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

Figure 28. Standby Mode Timing (can be used for single conversions)



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{12}(1)	Data ready after exiting Standby mode and calibration	78.8	79.7	ms

(1) Values given for f_{CLK} = 2MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

Figure 29. Standby Mode with Self-Calibration Timing (can be used for single conversions)

SINGLE CONVERSIONS

When only single conversions are needed, Standby mode can be used to start and stop the ADS1224. To make a single conversion, first enter the Standby mode holding SCLK high. Now, when ready to start the conversion, take SCLK low. The ADS1224 wakes up and begins the conversion. Wait for $\overline{\text{DRDY}}$/DOUT to go low, and then retrieve the data. Afterwards, take SCLK high to stop the ADS1224 from converting and re-enter Standby mode. Continue to hold SCLK high until ready to start the next conversion. Operating in this fashion greatly reduces power consumption since the ADS1224 is shut down while idle between conversions. Self-calibrations can be performed prior to the start of the single conversions by using the waveform shown in Figure 29.

APPLICATIONS INFORMATION

GENERAL RECOMMENDATIONS

The ADS1224 is a high-resolution A/D converter. Achieving optimal device performance requires careful attention to the support circuitry and printed circuit board (PCB) design. Figure 30 shows the basic connections for the ADS1224. As with any precision circuit, be sure to use good supply bypassing capacitor techniques. A smaller value ceramic capacitor in parallel with a larger value tantulum capacitor works well. Place the capacitors, in particular the ceramic ones, close to the supply pins. Use a ground plane and tie the ADS1224 GND pin and bypass capacitors directly to it. Avoid ringing on the digital inputs. Small resistors (≈100Ω) in series with the digital pins can help by controlling the trace impedance. Place these resistors at the source end.

Pay special attention to the reference and analog inputs. These are the most critical circuits. Bypass the voltage reference using similar techniques to the supply voltages. The quality of the reference directly affects the overall accuracy of the device. Make sure to use a low noise and low drift reference such as the REF1004.

Often, only a simple RC filter is needed on the inputs. This circuits limits the higher frequency noise. Avoid low-grade dielectrics for the capacitors and place them as close as possible to the input pins. Keep the traces to the input pins short, and carefully watch how they are routed on the PCB.

After the power supplies and reference voltage have stabilized, issue a self-calibration command to minimize offset and gain errors.

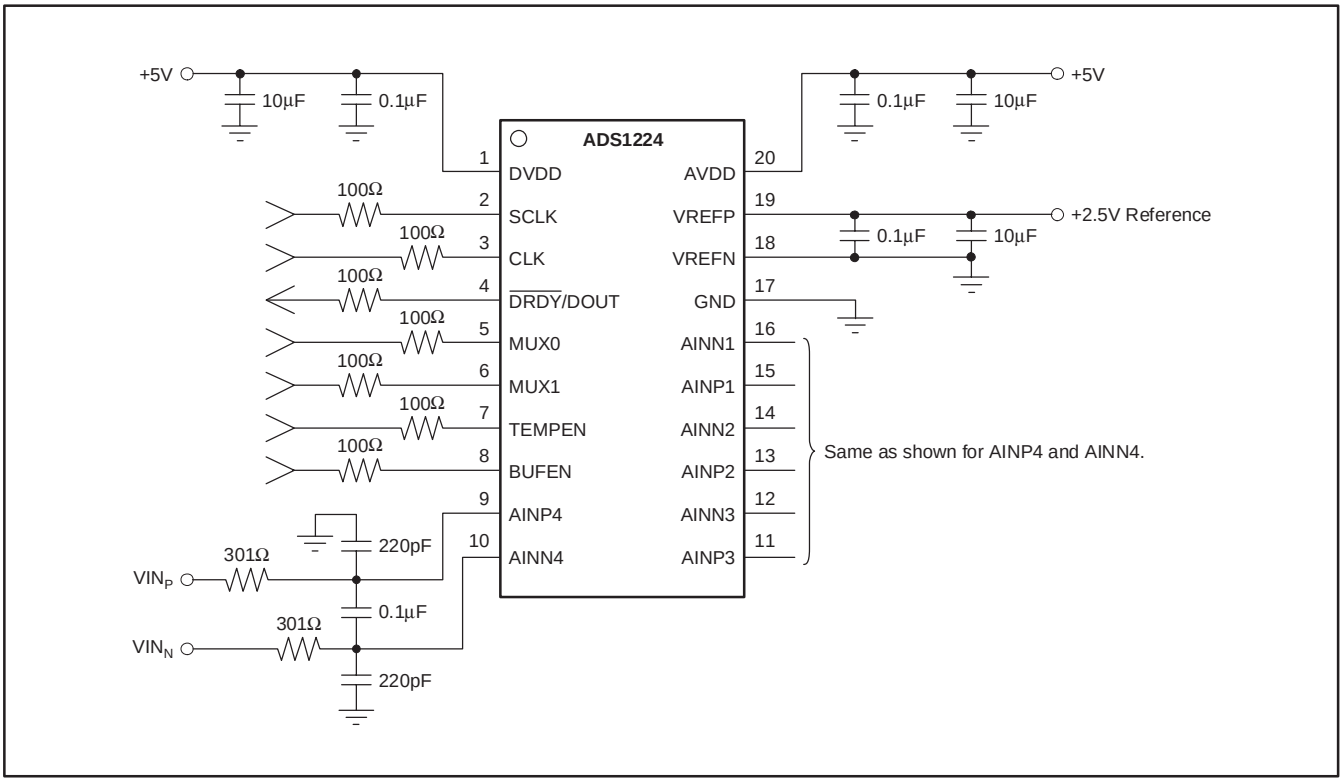


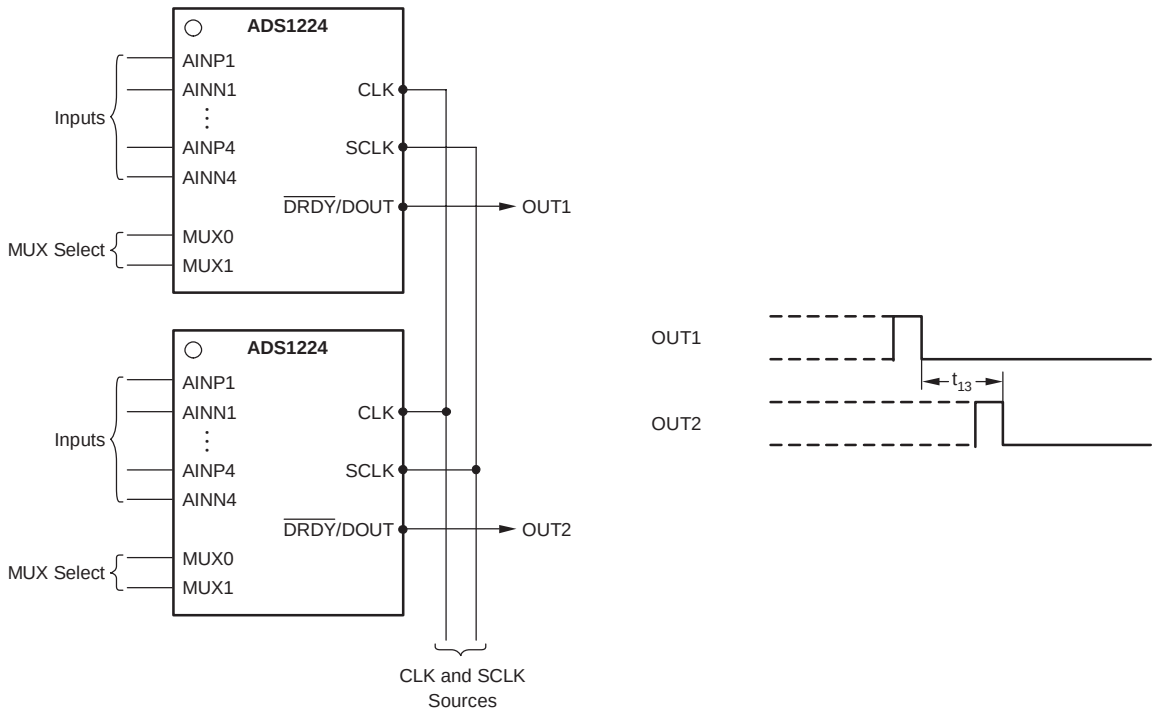
Figure 30. Basic Connections

MULTICHANNEL SYSTEMS

Multiple ADS1224s can be operated in parallel to measure multiple input signals. Figure 31 shows an example of an eight-channel system. For simplicity, the supplies and reference circuitry are not shown. The same CLK signal should be applied to all devices. To synchronize the ADS1224s, connect the same SCLK signal to all devices. Then place all the devices in Standby mode. Afterwards, starting a conversion will synchronize all the ADS1224s; that is, they will sample the input signals simultaneously. The $\overline{\text{DRDY}}$/DOUT outputs will go low at approximately the same time after synchronization. When reading data from the devices, the data appears in parallel on $\overline{\text{DRDY}}$/DOUT as a result of the common SCLK connection.

The falling edges of $\overline{\text{DRDY}}$/DOUT, indicating that new data is ready, will vary with respect to each other no more than time t_{13}. This variation is due to possible differences in the ADS1224 internal calibration settings. To account for this, when using multiple devices, either wait for t_{13} to pass after seeing one $\overline{\text{DRDY}}$/DOUT go low, or wait until all $\overline{\text{DRDY}}$/DOUTs have gone low before retrieving data.

Note that changing channels (using the MUX0 and MUX1 pins), or using the input buffer (BUFEN) or the temperature sensor (TEMPEN), may require more care to settle the digital filter. For example, if the MUX0 pin is toggled on one device and not the other, the $\overline{\text{DRDY}}$/DOUT line will be held high until the conversion settles on the first device. The latter device will continue conversions through this time. See the *Settling Time* section of this data sheet for further details.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{13}(1)	Difference between $\overline{\text{DRDY}}$/DOUTs going low in multichannel systems		±0.8	ms

(1) Values given for f_{CLK} = 2MHz. For different f_{CLK} frequencies, scale proportional to CLK period.

Figure 31. Example of Using Multiple ADS1224s in Parallel

VESSEL WEIGHING WITH FOUR LOAD CELLS

In vessel weighing systems, four load cells are frequently employed to measure the weight of the vessel and its contents. The output of the load cells are usually combined in an external summing junction box that balances the load cells' sensitivities for accuracy.

The four differential inputs of the ADS1224 allow for direct measurement of the four load cells individually. In this way, the mechanical adjustments performed inside the summing junction box are eliminated and are replaced by digital summing of the load cells in software. Figure 32 shows an example of such a system.

The reference voltage of the ADS1224 is derived by dividing down the AVDD supply voltage to 2.5V, while the load cell has a positive full-scale output of 10mV. In the figure, a low drift, dual op amp (OPA2335) provides a differential in/differential out amplifier with a gain of 499V/V ($G = 1 + 2R_F/R_G$). Gain on the load cell gives the amplifier a full-scale output of 5V.

Each load cell input uses an external amplifier. The outputs of the amplifiers connect to the analog inputs of the ADS1224 through a low-pass filter. The cut-off frequency is set to 360Hz, allowing full settling in a single measurement cycle. A lower cut-off frequency can be used to reduce noise from mechanical vibrations, but at the expense of filter settling time.

The internal buffer of the ADS1224 is disabled, allowing the VREFN pin to be grounded. Note that the loading from the reference inputs will change the effective reference voltage. The effective input impedance into the VREFP and VREFN pins will lower the reference voltage seen at these pins. At 2MHz, input impedance is approximately 500kΩ. For the reference circuit shown in Figure 32, this lowers the effective reference voltage by approximately 0.1%.

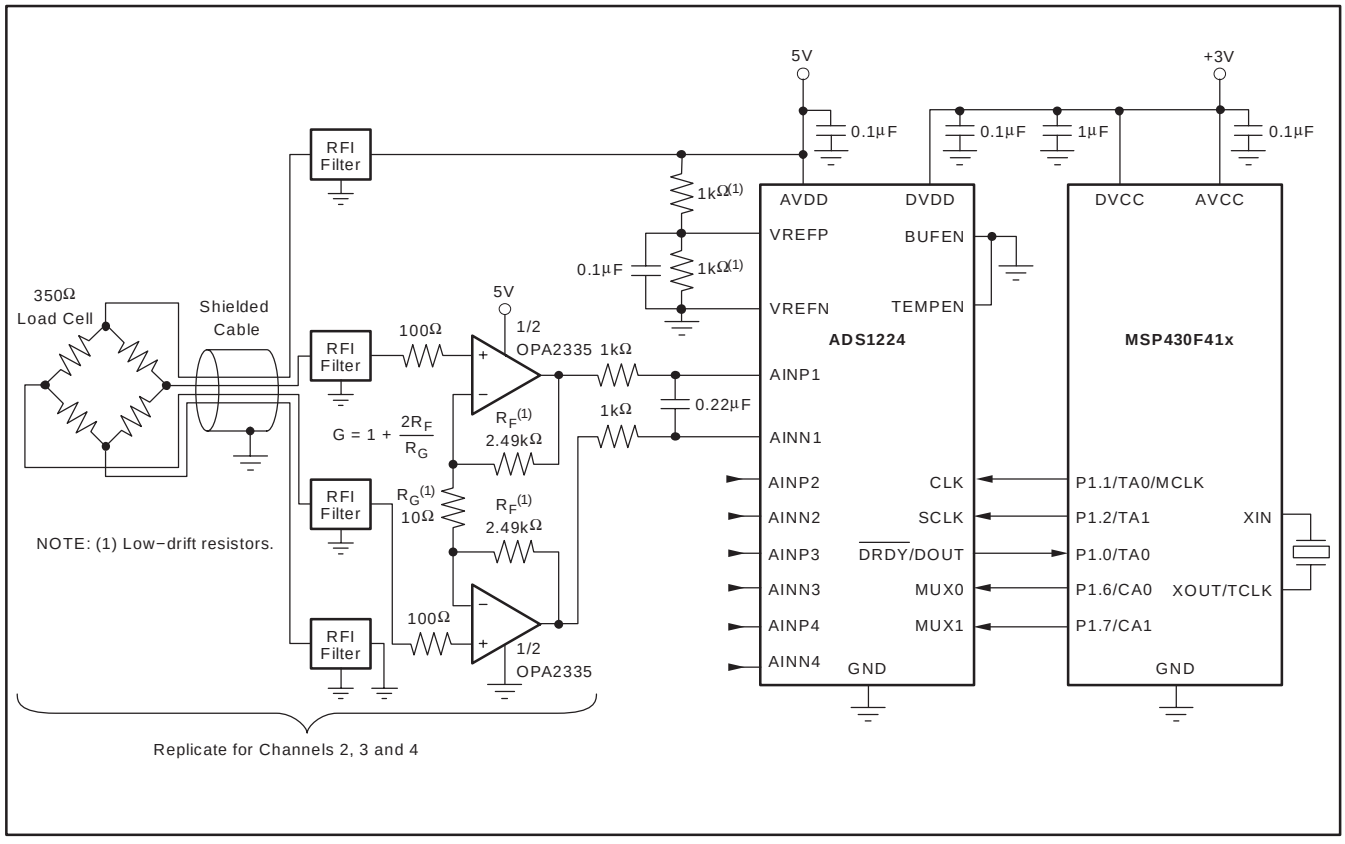


Figure 32. Vessel Weighing System with Four Load Cells

SUMMARY OF SERIAL INTERFACE WAVEFORMS

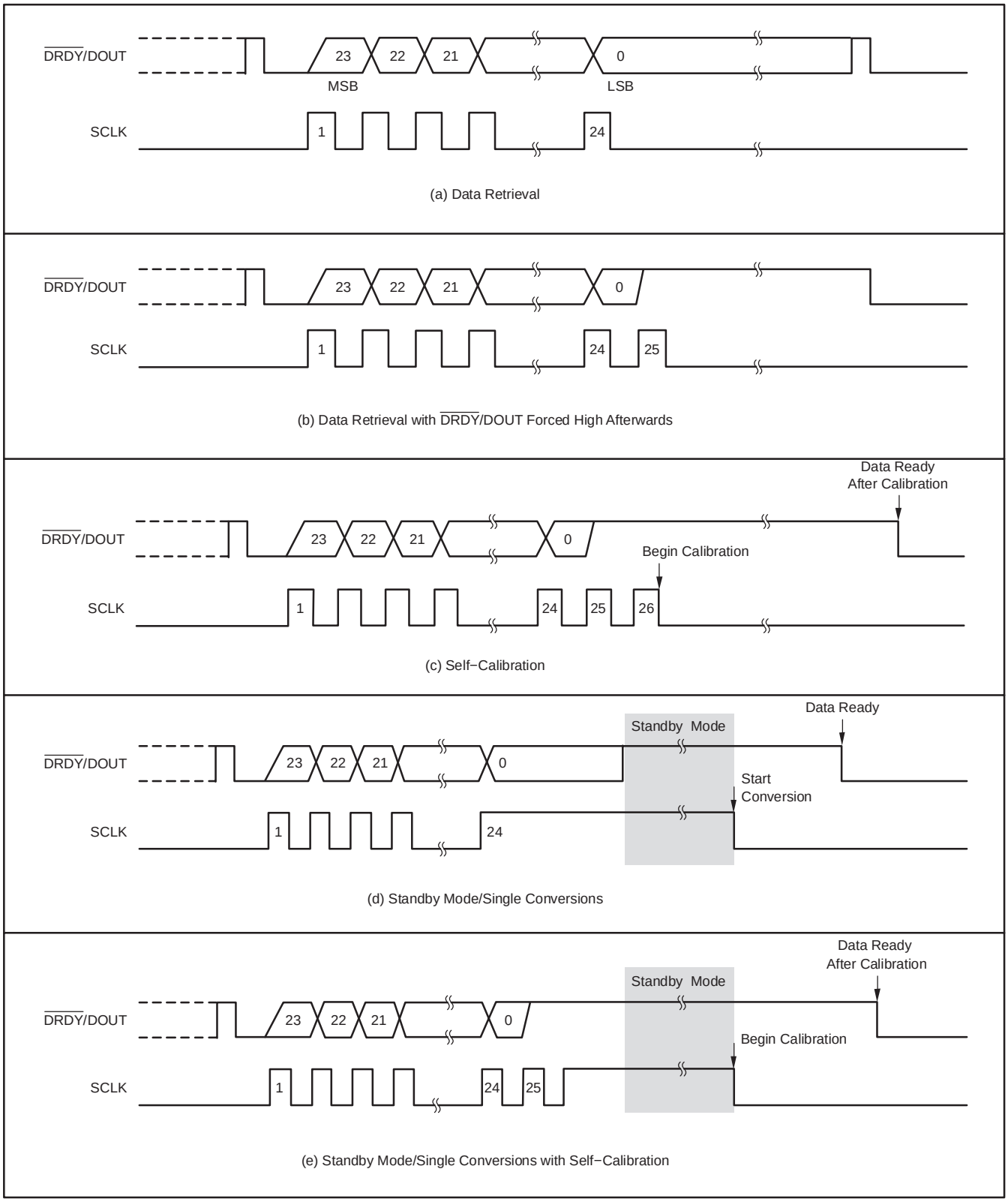


Figure 33. Summary of Serial Interface Waveforms

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
12/2/08	C	9	Analog Input Measurement with the Input Buffer	Added last sentence to first paragraph describing standby mode.
		15	Standby Mode	Added last sentence to first paragraph describing standby mode.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1224IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1224IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1224IPWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1224IPWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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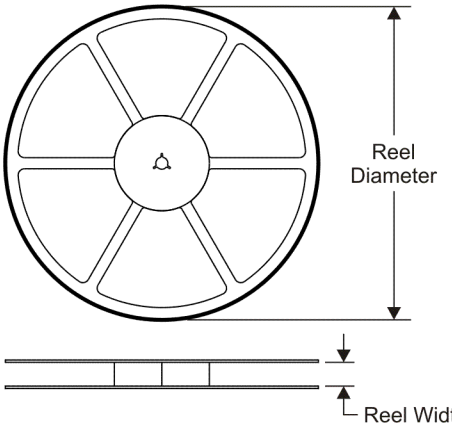
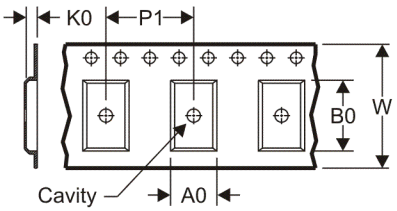
TAPE AND REEL INFORMATION

REEL DIMENSIONS

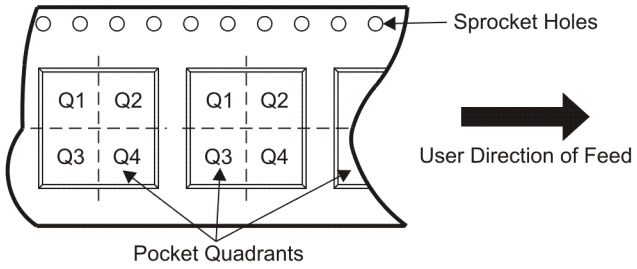


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

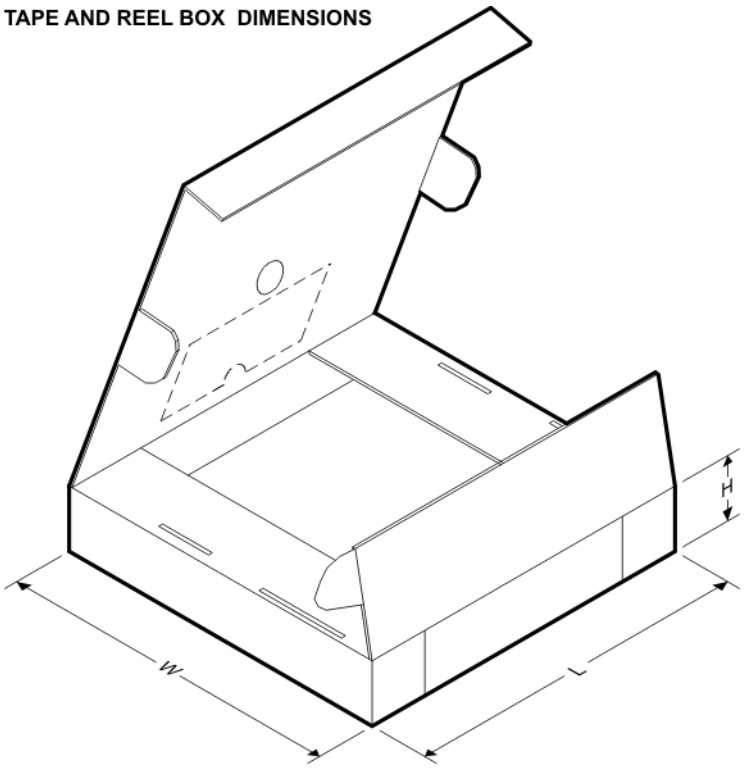
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1224IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
ADS1224IPWT	TSSOP	PW	20	250	180.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

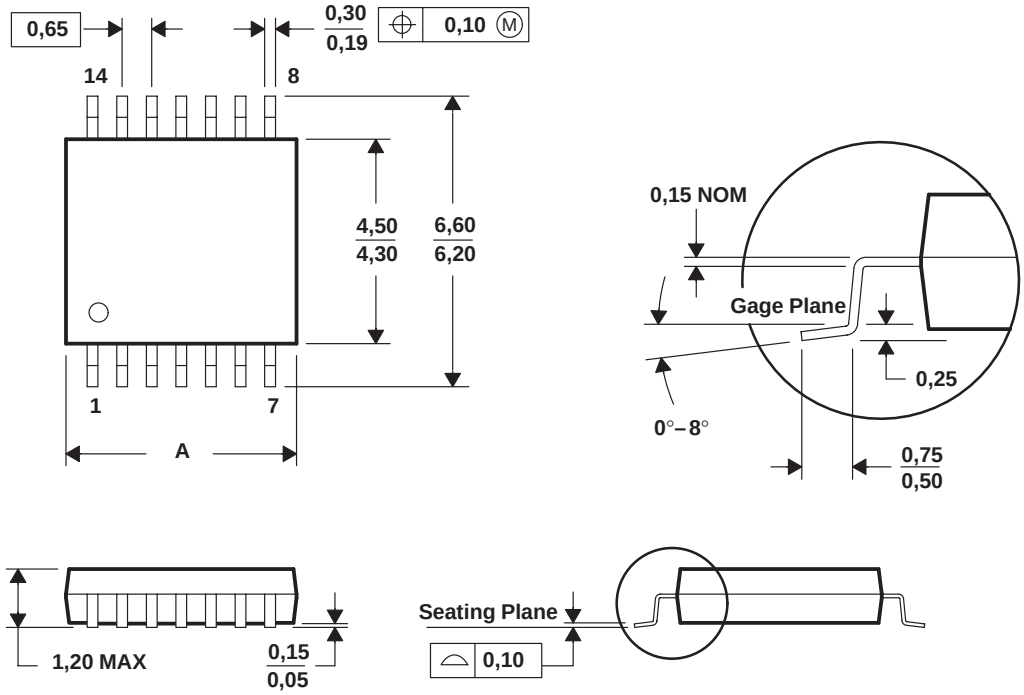


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1224IPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
ADS1224IPWT	TSSOP	PW	20	250	190.5	212.7	31.8

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS1224IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1224	Samples
ADS1224IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1224	Samples
ADS1224IPWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1224	Samples
ADS1224IPWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1224	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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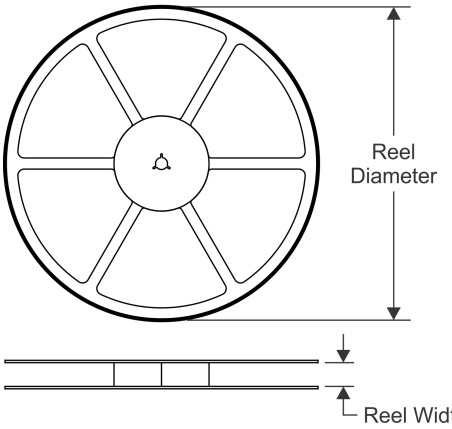
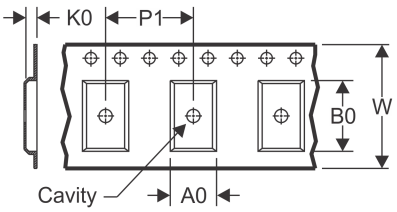
TAPE AND REEL INFORMATION

REEL DIMENSIONS

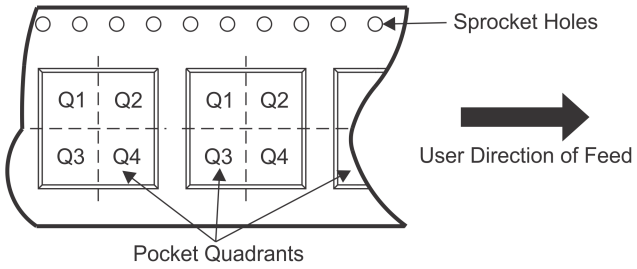


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

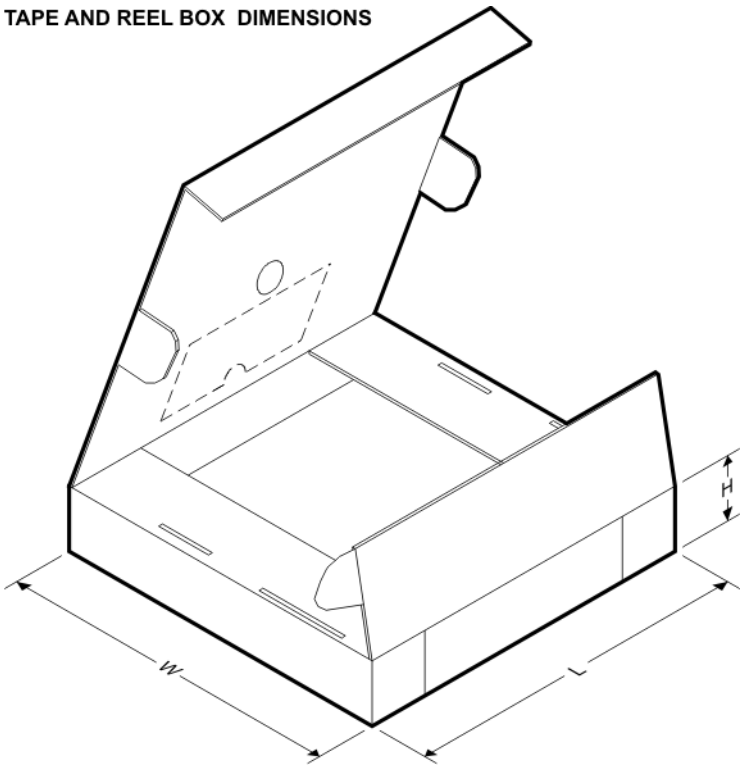
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1224IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
ADS1224IPWT	TSSOP	PW	20	250	180.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

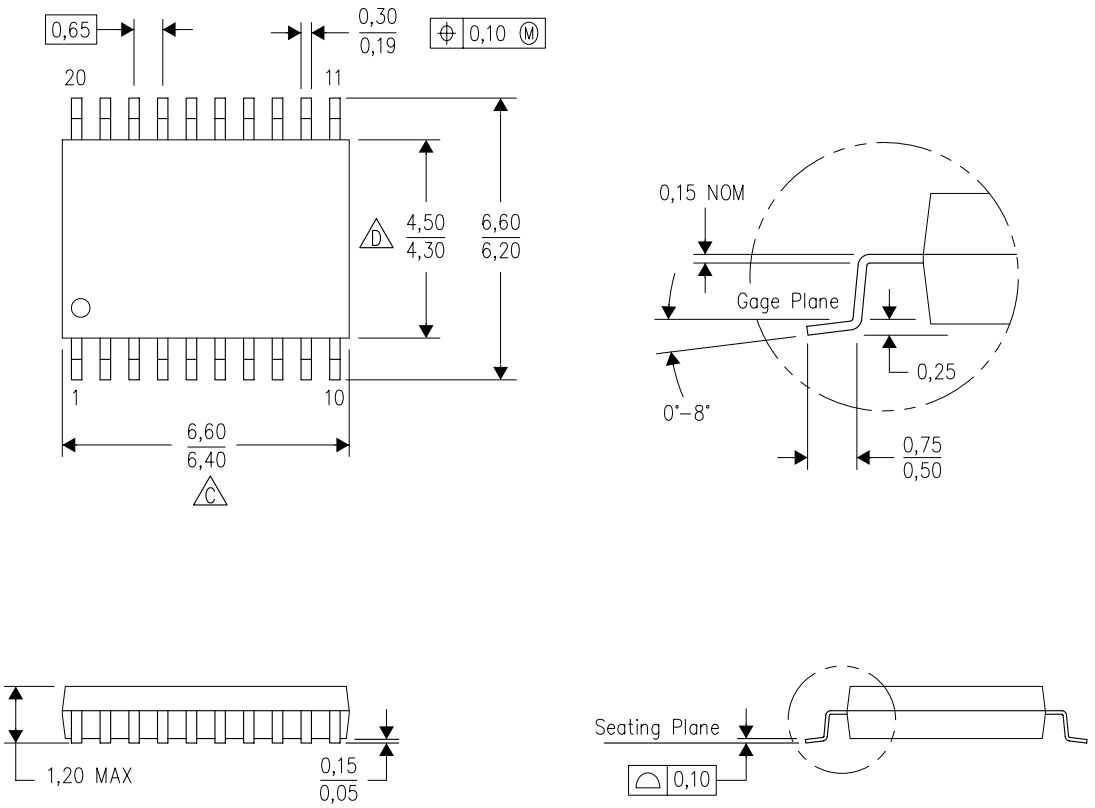
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1224IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
ADS1224IPWT	TSSOP	PW	20	250	210.0	185.0	35.0

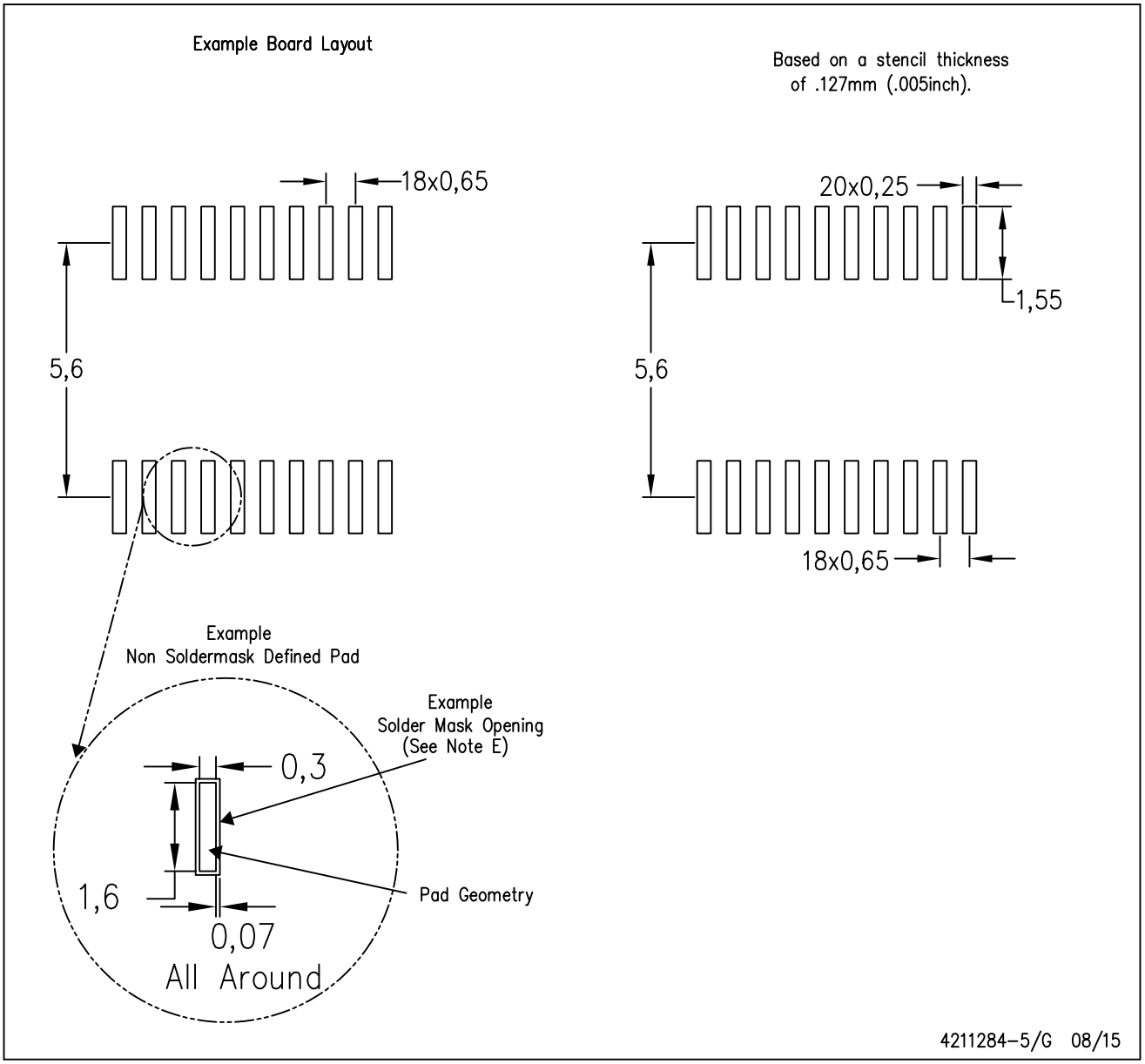
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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